ABSTRACT OF THE DISCLOSURE

A delay compensation circuit that determines the effects of process, voltage, and temperature (PVT) conditions of a chip by measuring the effective delay time of delay components inside the chip. The delay compensation circuit includes a plurality of sampler modules, each of which receives a delayed clock signal from one of a series of delay cells within a tapped delay circuit. The delay compensation circuit generates an output value based on the total number of sampling modules that lock into a fixed input signal using the delayed clock signals. Since the delay time of each delay cell changes based on variations of PVT conditions, the output values generated by the delay compensation circuit are determinate of PVT conditions in the chip. These output values can be used to design components to compensate for variances in PVT conditions or to control a variable delay component based on detected PVT conditions.